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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/960,007	09/20/2001	Mark T. Feuerstraeter	42390P10687	4223

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EXAMINER	
WONG, WARNER	
ART UNIT	**PAPER NUMBER**
2661	

DATE MAILED: 09/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/960,007	FEUERSTRAETER ET AL.	
	Examiner	Art Unit	
	Warner Wong	2661	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE ____ MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) *17-24* is/are withdrawn from consideration.

5)☐ Claim(s) _ is/are allowed.

6)☒ Claim(s) *1-3 and 5-15* is/are rejected.

7)☒ Claim(s) *4 and 9* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20-Sep-2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Restriction to one of the following inventions is required under 35 U.S.C. 121:

   I. Claims 1-16, drawn to adaptive systems, classified in class 370, subclass 465.

   II. Claims 17-24, drawn to synchronization including delay device, classified in class 465, subclass 517.

2. Inventions I and II are related as combination and subcombination. Inventions in this relationship are distinct if it can be shown that (1) the combination as claimed does not require the particulars of the subcombination as claimed for patentability, and (2) that the subcombination has utility by itself or in other combinations (MPEP § 806.05(c)). In the instant case, the combination as claimed does not require the particulars of the subcombination as claimed because it may use other sources for data synchronization. The subcombination has separate utility such as synchronization for a local clock.

3. Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their different classification, restriction for examination purposes as indicated is proper.

4. During a telephone conversation with Ed Talyor on August 16, 2005 a provisional election was made without traverse to prosecute the invention of Feuerstraeter, claims 17-24. Affirmation of this election must be made by applicant in replying to this Office action. Claims 17-24 withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

Drawings

5. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: #381 and #391 missing from figure 3, per the specification paragraph 39. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

6. The disclosure is objected to because of the following informalities:

In paragraph 42, the reference sign of #440 for frequency configuration unit should be #425. In paragraph 49, the reference sign of #502 for CMU should be #510.

Appropriate correction is required.

Claim Objections

7. Claim 9 is objected to because of the following informalities: There is no preceding reference to the first mention of "the frequency configuration unit". The word "the" should be changed to "a".

Also, "the data rate serial input" has no preceding reference. The word "serial" should be changed to "selector". Appropriate correction is required.

8. Claim 16 is objected to because of the following informalities: Grammatical error of singularity / plurality in the phrase: ".. a reference clock frequencies ..". Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 1, 11, 12 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mulaney ("518) in view of Walsh (4,890,316).

Regarding claim 1, Mulaney ('518) describes a circuitry that recovers (detects) 1 data signal rate (col. 7, lines 55-58), selects external reference clock corresponding to the data rate (fig. 5b, REF(WCLK) col. 11, lines 41-45), frequency and phase lock to the data (col. 11, lines 20-23 describing fig. 5b, #58 & 86), and (automatically) configures a serializer (col. 6, lines 46-48).

Mulaney ('518) fails to describe the circuitry capable of detecting (multiple) data rates.

Walsh ('316) describes a circuitry that detects multiple incoming data (baud) rates from a serial input (col. 13, lines 64-68).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify the circuitry of Mullaney ('202) to incorporate incoming data rate detection of Walsh ('316) so that it may be more versatile by supporting multiple data rates.

Regarding claim 11, Mulaney ('518) describes a circuitry with buses (connections within in fig. 5b), a connecting Port Logic (CPU) (fig. 5b, #56; col. 11, lines 27-33) with word generator and comparator (inherent with memory) (fig. 5b, #100; col. 13, lines 34-37), a connecting serializer/deserializer (fig. 5b, #60, #62), a Data Recovery Unit (DRU) (fig. 5b, #86) for recovering (sampling and receiving) 1 incoming data rate (combined data rate detection unit and first frequency configuration unit) (col. 7, lines 55-58), and a timing generator (fig. 5b, #96) (first frequency selector unit) for selecting a frequency from a connecting external clock/oscillator (fig. 5b, EXT(WCLK)).

Mulaney ('518) fails to describe the DRU capable of detecting (multiple) data rates.

Walsh ('316) describes a circuitry which detects multiple incoming data (baud) rates (col. 13, lines 64-68).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify the circuitry of Mullaney ('202) to incorporate incoming data rate detection of Walsh ('316) so that it may be more versatile by supporting multiple data rates.

Regarding claim 12, Mulaney ('518) describes the switch port (fig. 5b, #54) deserializer portion with a DRU (fig. 5b, #86) (combined first frequency configuration unit and first phase lock unit) phase locking the incoming signal (col. 11, lines 20-23).

The DRU (first frequency configuration unit) inside the Switch Port (fig. 5b, #54) has a connection (data rate select output) to the CRU (fig. 5a, #80) (second frequency configuration unit) in transceivers (fig. 4, #52) as part of a transmit/receive clock feedback loop (col. 11 lines 66-67 and col. 12, lines 1-6). The DRU also phase locks the incoming signal (col. 11, lines 20-23).

Regarding claim 16, Mulaney ('518) describes the CRU (fig. 5a, #80) (second frequency configuration unit) in transceivers (fig. 4, #52) having a connection (data rate selector input) (fig. 5a, RXS line) to the DRU (first frequency configuration unit) in switch port (fig. 4, #54) as part of a transmit/receive clock feedback loop (col. 11 lines 66-67 and col. 12, lines 1-6), and a timing generator (fig. 5b, #98) (second frequency selector unit) selecting a frequency from the external connecting oscillator (fig. 5b, EXT(WCLK)).

10. Claims 2, 5-6, 8, 13 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mulaney ('518) and Walsh ('316), and further in view of Stuttard (4,270,202).

Regarding claim 2, Mulaney ('518) fails to describe the serializer with time delay for configuring from a LAN to WAN mode.

Stuttard ('202) describes a multiplexing modem (serializer) (col. 3, lines 21-24, fig. 1, #11) configured by time delay units (fig. 1, #21) in support of dynamic (automatic)

port mode changes (col. 1, lines 52-65) for adjusting to various channel data rate (and col. 4, lines 40-45).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify the circuitry of Mullaney ('202) to incorporate the time delay and port mode/rate changes of Stuttard ('202) so that it may be more versatile by supporting differing modes/rates, including LAN and WAN rates.

Regarding claim 5, Mulaney ('518) describes a DRU (combined data rate detection unit and first frequency configuration unit) (fig. 5b, #86) for recovering (sampling) and receiving 1 detected data rate (col. 7, lines 55-58), as well as connecting timing generator (fig. 5b, #96) (frequency selector unit) for selecting a frequency from a connecting external clock/oscillator (fig. 5b, REF(WCLK), col. 41-45).

The DRU (first frequency configuration unit) inside the Switch Port (fig. 5b, #54) has a connection (data rate select output) to the CRU (fig. 5a, #80) (second frequency configuration unit) in transceivers (fig. 4, #52) as part of a transmit/receive clock feedback loop (col. 11 lines 66-67 and col. 12, lines 1-6). The DRU (phase lock unit) also phase locks the incoming signal (col. 11, lines 20-23).

Walsh ('316) describes a modem which detects multiple incoming data (baud) rates (col. 13, lines 61-67).

Mullaney ('518) and Walsh ('316) fail to describe an oscillator to generate a plurality of reference clock frequencies and a frequency selector unit to select one of the reference clock frequencies.

Stuttard ('202) describes a clock/oscillator (fig. 2, #105) generating four (plurality) clock reference signals (col. 3, lines 53-57) and a clock (frequency) selection unit (fig. 2, #101) to select the frequency references (col. 3, lines 50-52).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify the circuitry of Mulaney ('518) and incorporate support of multiple transceiving frequencies from Walsh ('316) and Stuttard ('202) so that it may support various data input rates.

Regarding claim 6, Stuttard ('202) describes time delay units (timers) to allow modems (configuration units) from detection to setup time of a new port mode/rate configuration (and col. 4, lines 46-54).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify the circuitry of Mullaney ('518) to incorporate the delay circuitry of Stuttard ('202) in support of the overall port mode/rate reconfiguration.

Regarding claim 8, Stuttard ('202) describes various supporting data signal frequencies in Table A (col. 4, lines 5-24), but not the LAN rate of approximately 10.31 GHz and the WAN rate of approximately 9.95GHz.

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify the system described in the 10GE Overview document and Stuttard ('202) to incorporate the LAN and WAN rates due to popularity in usage.

Regarding claim 13, Mulaney ('518) describes a serializer/deserializer in the switch circuit (chipset).

Mulaney fails to describe a timer delay.

Stuttard ('202) describes time delay units (timers) to allow modems (configuration units) from detection to setup time of a new port mode/rate configuration (and col. 4, lines 46-54).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify the circuitry of Mullaney ('518) to incorporate the delay circuitry of Stuttard ('202) in support of the overall port mode/rate reconfiguration.

Regarding claim 15, Melaney ('518) fails to describe the frequency that phase locks the incoming signal can be selectable and consists of approximately 10.31 GHz and 9.95 GHz.

Stuttard ('202) lists the phase frequencies generated for the transmit circuitry in Table A (col. 4, lines 5-24), but not the LAN rate of approximately 10.31 GHz and the WAN rate of approximately 9.95GHz.

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify the system described by Melaney ('518) and Stuttard ('202) to support multiple data rates, especially LAN and WAN rates due to popularity in usage.

11. Claims 3, 7 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mulaney ('518), Walsh ('316) and Stuttard ('202) as applied to claim 2 above, and further in view of Hoefelmeyer (6,385,204).

Regarding claim 3, Mulaney ('518) , Walsh ('316) and Stuttard ('202) describe a serializer configured by time delay units for responding and setting up mode changes (col. 4, lines 46-50).

Mulaney ('518), Walsh ('316) and Stuttard ('202) fail to describe the time delay period equaling 1.6 milliseconds.

Hoefelmeyer ('204) stated that it has been proven that real-time latencies across the WAN to be approximately 1.6 milliseconds (col. 15, lines 59-62).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to specify an arbitrary time delay period to be equal or greater than 1.6 milliseconds in changing the mode to the approximate WAN rate.

Regarding claim 7, Studdard ('202) describes a timer delay.

Stuttard ('202) fail to describe the time delay period equaling 1.6 milliseconds.

Hoefelmeyer ('204) stated that it has been proven that real-time latencies across the WAN to be approximately 1.6 milliseconds (col. 15, lines 59-62).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to specify an arbitrary time delay period to be equal or greater than 1.6 milliseconds in changing the mode to the approximate WAN rate.

Regarding claim 14, Studdard ('202) describes a timer delay.

Stuttard ('202) fail to describe the time delay period equaling 1.6 milliseconds.

Hoefelmeyer ('204) stated that it has been proven that real-time latencies across the WAN to be approximately 1.6 milliseconds (col. 15, lines 59-62).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to specify an arbitrary time delay period to be equal or greater than 1.6 milliseconds in changing the mode to the approximate WAN rate.

12. Claims 9-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mulaney ('519) in view of Stuttard ('202).

Regarding claim 9, Mulaney ('518) describes a Clock Recovery Unit (CRU) (fig. 5a, #80) (second frequency configuration unit) in transceivers (fig. 4, #52) having a connection (data rate selector input) to the Data Recovery Unit (DRU) (fig. 5b, #86) (first frequency configuration unit) in switch port (fig. 4, #54) as part of a transmit/receive clock feedback loop (col. 11 lines 66-67 and col. 12, lines 1-6), as well as a timing generator (fig. 5b, #96) (frequency selector unit) for selecting a frequency from a connecting external clock/oscillator (fig. 5b, #58).

Mulaney ('518) fails to describe the CRU (frequency selector unit) able to select various frequencies generated by the external oscillator.

Stuttard ('202) describes a clock/oscillator (fig. 2, #105) generating four (plurality) clock reference signals (col. 3, lines 53-57) and a clock (frequency) selection unit (fig. 2, #101) to select the frequency references (col. 3, lines 50-52).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify the circuitry of Mulaney ('518) and incorporate the units supporting multiple clock frequencies of Stuttard ('202) so that it may support various data input rates.

Regarding claim 10, Stuttard ('202) describes the phase frequencies generated for the transmit circuitry in Table A (col. 4, lines 5-24), but not the LAN rate of approximately 10.31 GHz and the WAN rate of approximately 9.95GHz.

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify the system described by Melaney ('518) and Stuttard ('202 to support multiple data rates, especially LAN and WAN rates due to popularity in usage.

Allowable Subject Matter

13. Claim 4 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

14. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Warner Wong whose telephone number is 571-272-8197. The examiner can normally be reached on 6:00AM - 3:00PM, M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chau Nguyen can be reached on 571-272-3126. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Warner Wong WW
Examiner
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